REMARKS

Applicant thanks the Examiner for the careful review of this application. Claims 1, 6 and 8-9 were amended to clarify aspects of the present invention. Claims 10-23 have been added. No new matter was added. Accordingly, Claims 1-23 are pending in this application.

CLAIM OBJECTIONS

Claims 1-5 and 6-8 were objected to because of various informalities. The claims have been amended to clarify aspects of the present invention.

Withdrawal of the claim objections is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 112, FIRST PARAGRAPH

Claims 1-8 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement. Applicant respectfully traverses these rejections.

Applicant's specification discloses that a time difference TM is adjustable. TM defines the time difference between CLK1/CLK2 and CLK2/CLK3. TM for the two regions is always equal but it is still adjustable such that a valid data region can accurately be maintained as the eye opening changes. That is, the whole distribution between CLK1 and CLK3 can be moved left or right and the value of TM can additionally be increased or decreased. This is fully described via Applicant's Fig. 3A and in the specification:

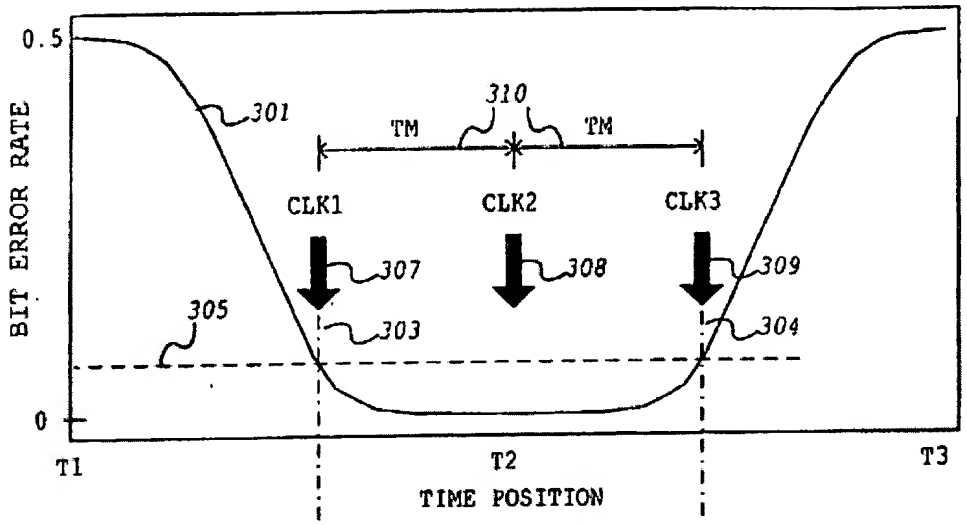


FIG. 3a

[0026] In the present invention, 'CLK2' 308 is controlled by a phase control signal that is determined from the difference of the bit-error-rate measured at 'CLK1' 307 and the one measured at 'CLK3' 309. 'CLK1' 307 and 'CLK3' 309 are advanced and delayed from 'CLK2' 308 by the time difference of 'TM' 310, respectively. The time difference 'TM' 310 is controlled by another phase control signal that is determined from the summation of the two bit-error-rate. If bit-error-rate at 'CLK1' 307 is greater than the one at 'CLK3' 309, it means that the overall sampling phase leads the eye opening. Therefore, the phase of 'CLK2' 308 is delayed until the two bit-error-rate becomes equal. On the contrary, if the bit-error-rate at 'CLK1' 307 is smaller, the phase of 'CLK2' 308 is advanced. If the sum of the two bit-error-rate exceeds a predetermined value, 'TM' 310 is decreased to shrink the sampling window to the eye opening. If the sum is less than predetermined value, 'TM' 310 is increased.

-Applicant's specification, paragraph 26

Dependent claims 10-13 reflect the above-described embodiment such that a plurality of sampling clocks and a time distance between a first-occurring clock

of the plurality of clocks and a last-occurring clock of the plurality of clocks is automatically adjustable.

Withdrawal of the rejections of claims 1-8 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102(b)

Claim 9 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,218,771 to Hogge (hereinafter "Hogge").

REJECTIONS UNDER 35 U.S.C. § 103(a)

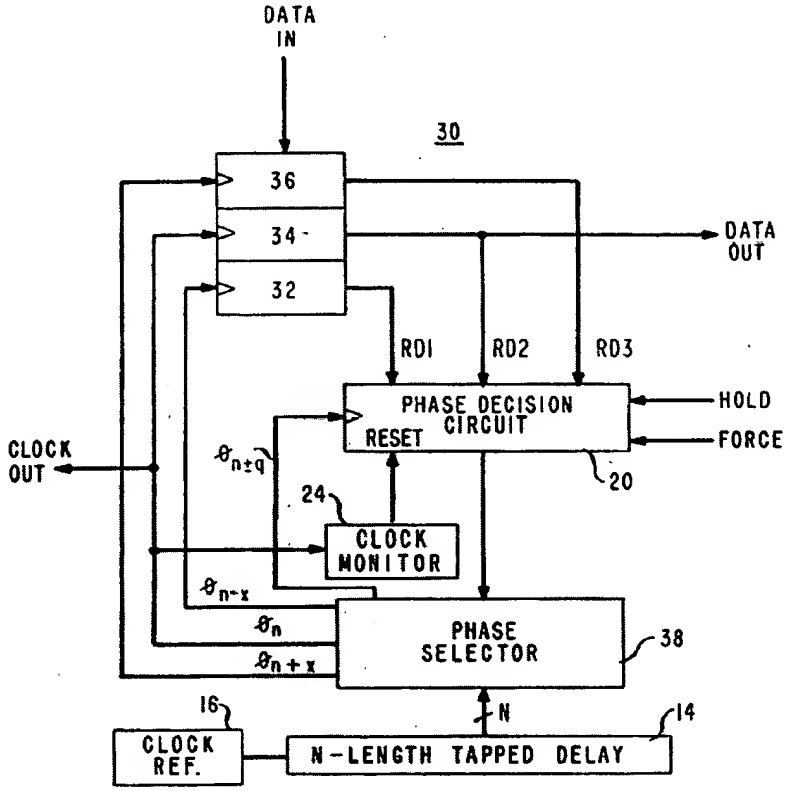
Claims 1-3 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,821,297 to Bergmann et al. (hereinafter "Bergmann") in view of Hogge.

Applicant respectfully traverses for the following reasons.

PRIOR ART

Bergman apparently discloses a digital clock recovery scheme. Included is reference clock used to provide a plurality of N signals with different clock phases. The incoming data stream is sampled and clocked with the reference clock to generate a plurality of M samples for each data bit. The logic values of the M samples are then analyzed to determine the relationship between the current clock phase and the data bit transition. If all samples agree, the clock phase is perhaps aligned with the data. If the clock phase is either leading or lagging the data, various samples will disagree. In the latter situation, the clock phase is adjusted until all samples agree, the particular clock which provides this state thus being defined as the recovered clock signal.

Bergman teaches that the analysis of the logic values is facilitated using a phase decision circuit. The phase decision circuit has three inputs and one output. To further illustrate, Figure 6 of Bergman is provided below:



As shown, RD1, RD2 and RD3 are provided as inputs to the phase decision circuit. The phase decision circuit compares the values of RD1, RD2, and RD3 to determine whether the current clock phase is correct or requires modification, as illustrated by the following excerpt:

> "In accordance with the teachings of the present invention, phase decision circuit 20 compares the values of RD1, RD2, and RD3 to determine

whether the current clock phase is correct or requires modification (incrementing or decrementing)." [Bergman, col. 3, lines 57-61]

Once determined, the phase decision circuit provides either a "no change," "decrement" or "increment" output signal to the phase selector as illustrated with the following excerpts:

"Presented with this '0-0-0' input, circuit 20 will now instruct selector 22 to maintain, or hold, the present clock phase, as long as the sampled data points continue to agree in value." [Bergman, col. 4, lines 42-45]

"The input '0-0-1' thus presented to decision circuit 20 will result in the generation of a 'decrement' output which is subsequently applied as an input to selector 22." [Bergman, col. 4, lines 25-28]

"The input of '1-0-0' to decision circuit causes circuit 20 to generate an 'increment' output, which is subsequently applied as an input to selector 22." [Bergman, col. 4, lines 49-53]

Hogue apparently discloses an automatic clock positioning circuit for positioning a clock pulse for a digital data stream that resembles an eye pattern when seen on an oscilloscope in response to digital data when the sweep is equal to the baud, bit or clock rate. Included in the circuit is a timing source for providing a stream of clock pulses and a controllable phase shift means electrically connected to said timing source and in response to an error signal will either advance, delay or maintain the phase of said stream of clock pulses. Also included is a pseudo-error indicator means for providing an upper, lower, early

and late boundary condition within the center of the eye pattern of the digital data stream and providing a first pseudo-error signal for each violation of the upper or lower boundary condition by the eye pattern at the early boundary condition and a second pseudo-error signal for each violation of the upper and lower boundary condition at the late boundary of the eye pattern, means for integrating the first and second error signals, means for comparing the integrated first error signal with the integrated second pseudo-error signal providing an error correcting signal; and means for controlling the controllable phase shift means with the error connecting signal.

Hogue teaches a clock positioning circuit that includes a voltage comparator. The voltage comparator receives an input signal and provides an output. To further illustrate, Figure 3 of Hogue is provided below:

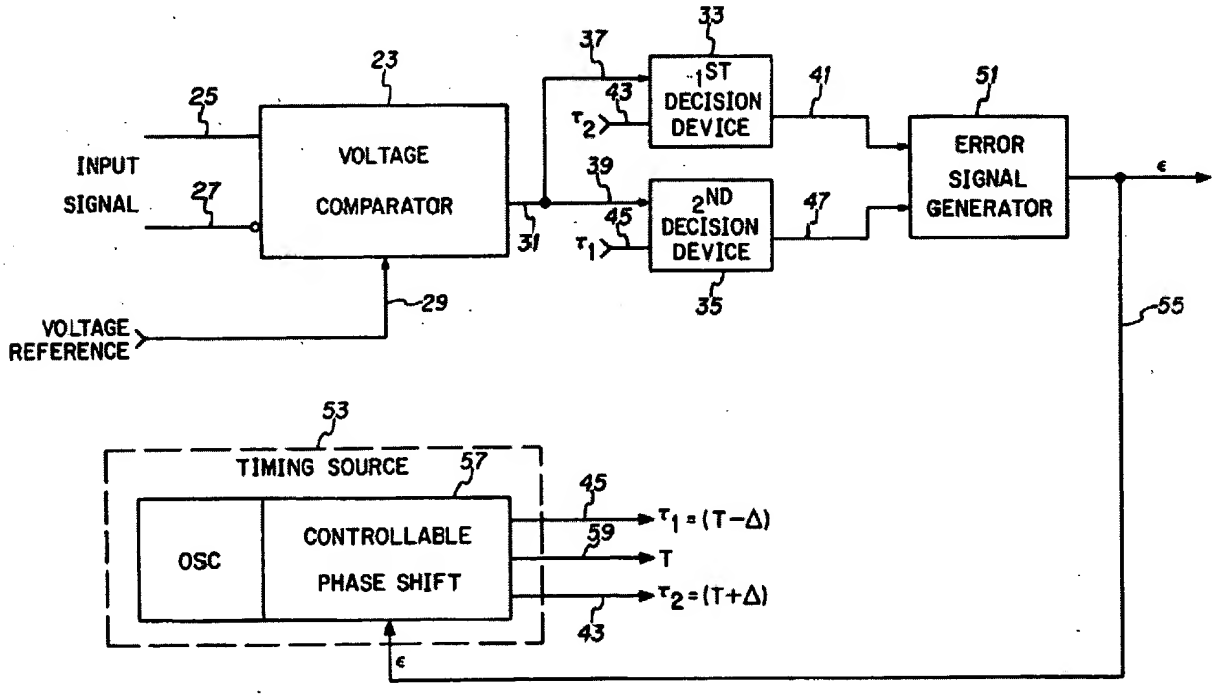


FIG. 3

As shown, an input signal is provided to the voltage comparator at terminals 25 and 27. The output of the voltage comparator is coupled to a first decision device and a second decision device. The output of the voltage comparator indicates whether boundary conditions have been transgressed, as illustrated by the following excerpt:

> "The output of the voltage comparator appears on terminal 31 and is coupled to a first decision device 33 and also to a second decision device 35 by means of conductors 37 and 39, respectively. The first decision device is used to indicate a pseudo-error when the output of the voltage comparator 23 indicates that there has been a transgression of the boundary conditions." [Hogue, col. 3, lines 56-63]

PRIOR ART DISTINGUISHED

As discussed above, Bregman teaches a phase decision circuit in which three data samples are received as inputs and a single output is provided to the phase selector. The single output to the phase selector corresponds to "no change," "decrement" or "increment." Hogue teaches a voltage comparer in which the input signal is received and a single output is provided. The single output of the voltage comparer corresponds to whether a boundary condition has been transgressed. Neither Bregman nor Hogue teaches compare logic that provides at least a first pseudo-bit error value and a second pseudo-bit error value. Further, neither Bregman nor Hogue teaches using the first and second pseudo-bit error values to estimate the phase relationship between the input data and a plurality of sampling clocks. Rather, Bregman teaches a single output from the phase decision circuit indicating "no change," "increment," or

"decrement." Hogue teaches a single output that indicates whether a boundary condition has been transgressed.

In contrast to Bregman and Hogue, amended Claim 1 contains the language, "at least a first pseudo-bit error value and a second pseudo-bit error value" and "phase controlling means for estimating the phase relationship between the input data and said plurality of sampling clocks using at least said first pseudo-bit error value and said second pseudo-bit error values." As discussed above, Bregman teaches a phase decision circuit having a single output corresponding to "no change," increment" or "decrement." Hogue teaches a voltage comparer having a single output corresponding to whether a boundary condition has been transgressed. Thus, neither Bregman nor Hogue teaches "at least a first pseudo-bit error value and a second pseudo-bit error value" and "phase controlling means for estimating the phase relationship between the input data and said plurality of sampling clocks using at least said first pseudo-bit error value and said second pseudo-bit error values." As such, the Examiner has not made a prima facie case of obviousness with respect to Claim 1. For at least these reasons, the independent Claim 1 is allowable over the teachings of Bregman and Hogue.

Claims 2-5 are either directly or indirectly dependent on the independent Claim 1. As described above, the independent Claim 1 is allowable over the teachings of Bregman and Hogue. Accordingly, Claims 2-5 are also at least allowable as being dependent on an allowable claim.

In contrast to Bregman and Hogue, amended Claim 6 contains the language, "at least a first pseudo-bit error value and a second pseudo-bit error value" and "a phase controller that estimates the phase relationship between the input data and said plurality of sampling clocks using at least said first pseudo-bit error value and said second pseudo-bit error value." As discussed above,

Bregman teaches a phase decision circuit having a single output corresponding to "no change," increment" or "decrement." Hogue teaches a voltage comparer having a single output corresponding to whether a boundary condition has been transgressed. Thus, neither Bregman nor Hogue teaches "at least a first pseudo-bit error value and a second pseudo-bit error value" and "a phase controller that estimates the phase relationship between the input data and said plurality of sampling clocks using at least said first pseudo-bit error value and said second pseudo-bit error values." As such, the Examiner has not made a prima facie case of obviousness with respect to Claim 6. For at least these reasons, the independent Claim 6 is allowable over the teachings of Bregman and Hogue.

Claims 7-8 are directly dependent on the independent Claim 6. As described above, the independent Claim 6 is allowable over the teachings of Bregman and Hogue. Accordingly, Claims 7-8 are also at least allowable as being dependent on an allowable claim.

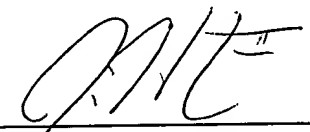
In contrast to Bregman and Hogue, amended Claim 9 contains the language, "providing a first pseudo bit-error signal from a comparer" and "providing a second pseudo bit-error signal from said comparer." As discussed above, Bregman teaches a phase decision circuit having a single output corresponding to "no change," increment" or "decrement." Hogue teaches a voltage comparer having a single output corresponding to whether a boundary condition has been transgressed. Thus, neither Bregman nor Hogue teaches "providing a first pseudo bit-error signal from a comparer" and "providing a second pseudo bit-error signal from said comparer." As such, the Examiner has not made a prima facie case of obviousness with respect to Claim 9. For at least these reasons, the independent Claim 9 is allowable over the teachings of Bregman and Hogue.

CONCLUSION

Applicant believes that all pending claims are allowable and a Notice of Allowance is respectfully requested. The amendment was made to expedite the prosecution of this application. Applicant respectfully traverses the rejections of the amended claims and reserves the right to re-introduce them and claims of an equivalent scope in a continuation application.

If the Examiner believes that a conference would be of value in expediting the prosecution of this application, he is cordially invited to telephone the undersigned counsel at the number set out below.

Respectfully submitted,
PERKINS COIE LLP



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